MSI-P450

ANALOG INPUT/OUTPUT CARD

USER MANUAL

PC/104 Embedded
Industrial Analog I/O Series

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I. INTRODUCTION

The MSI-P450 series is a low cost, high performance analog I/O board providing four 12-bit analog input channels and up to four 16-bit analog output channels. The board is designed for use with all PC/104 embedded systems. Eight models provide from 1 to 4 analog outputs with or without 4 analog single-ended inputs. Analog input channels are each selectable for 0-5V or 0-10V with a maximum non-linearity of ±1 LSB. Each analog output channel is selectable for 0-10V, ±5V or ±10V with a maximum non-linearity of ±6 LSB. The card operates from a single +5V supply. A block diagram of the card is shown in Fig. 1.

The card employs an ADS7842E for A/D inputs and up to four DAC7741Y for D/A outputs. Potentiometers are provided for adjustment of the offset and gain of each analog output. Single 10-pin connectors are provided for the analog inputs and the analog outputs.

The card is I/O mapped using 16-bit addressing to select the input channels and device status. Option jumpers

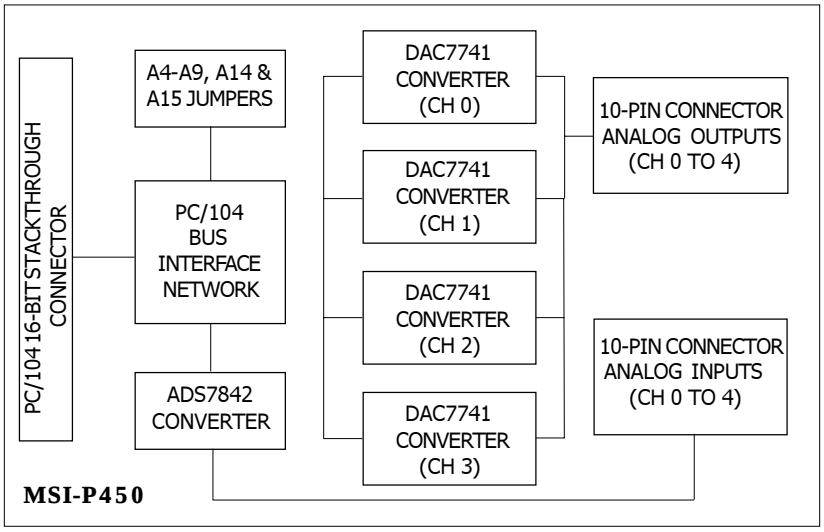

Figure 1. Block Diagram of the MSI-P450.

are provided for specifying the card base addresses A4 thru A9, A14 and A15. I/O reads and writes are 16 bits in length for efficient software sequences for acquiring data., as described in the next section.

II. HARDWARE DESCRIPTION

A. Card Configuration

The MSI-C450 card is a CMOS design using through-hole and surface-mounted devices. The card configuration is shown in Figure 2 and a circuit diagram of the network is given in the Appendix. The input signals for analog input channels 0 thru 3 are applied to connector J2. These signals are directed to the input terminals of A/D converter U14 (Ch. 0-3). Input range selection is provided by jumpers installed on JP6 for each input channel.

Analog output channels 0 thru 3 are applied to J1. These signals are directed to the output terminals of D/A converters

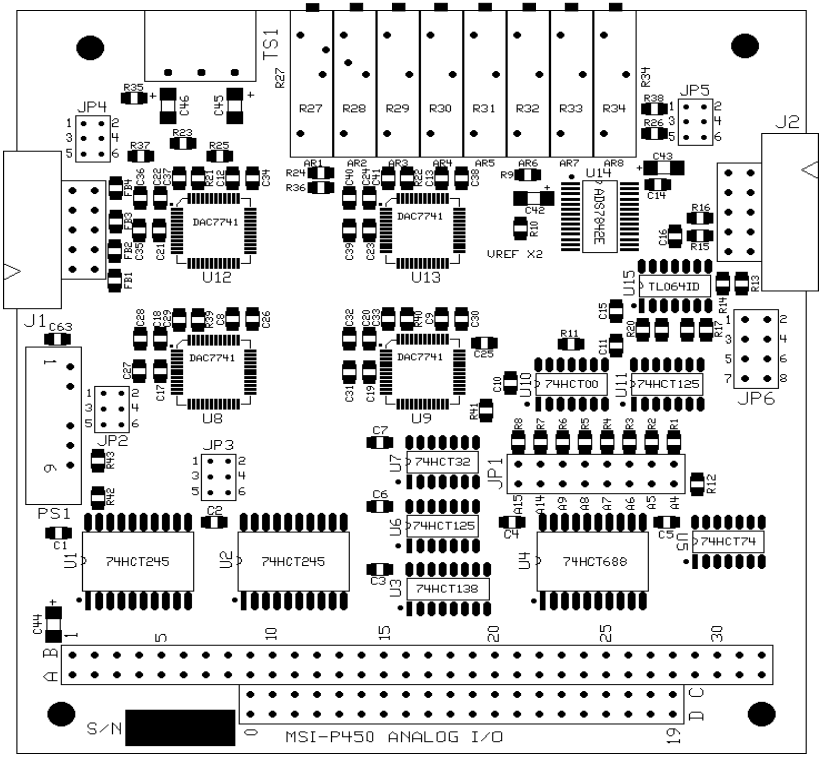

Figure 2. MSI-P450 card outline.

U8 (Ch. 0), U9 (Ch. 1), U12 (Ch. 2) and U13 (Ch. 3). Output range selection is provided by jumpers installed on JP2 thru JP5, respectively, for output channels 0 thru 3.

Jumper block JP1 is used for the card base address selection (Pins 1 thru 16) , as described below.

B. Card Addressing

The card I/O Base Address is set by installing appropriate jumpers on JP1, pins 1 thru 16, as shown in Figure 3. An uninstalled jumper for a given address bit sets the bit to 0 (false) and an installed jumper sets the bit to 1 (true). I/O addresses A4 thru A9, A14 and A15 are jumper selectable for defining the *Base Address* of the card from 0000H to FFFFH on integral 8H boundaries, where H denotes a hexadecimal number. The card I/O addresses will be imaged in addresses 400H thru 3C00 since A10 thru A13 are not decoded by the card.

To assign a Base Address of 8200H, for example, install jumpers JP1-5,6 (A9) and JP1-1,2 (A15).

C. Analog Output Channels .

1. Analog Output Range Selection.

The analog output channels have three selectable ranges of 0-10V, ±5V or ±10V installing 2mm jumpers on JP2 thru JP5 for channels 0 (DAC0) thru 3 (DAC3) as shown

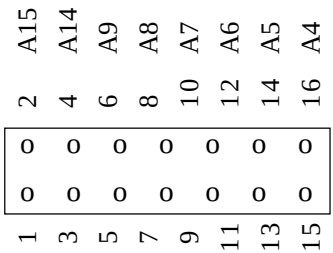

Figure 3. Jumper block JP1 configuration.

in Table 1 for each channel.

Table 1. Output Range Selection Using JP2 thru JP5.

RANGE	INSTALL JUMPERS
0-10V	1,2 & 5,6
±5V	3,4 & 5,6
±10V	NONE

2. Analog Output Values.

The analog outputs are are set by I/O word writes in offset binary to the desired output address. The outputs are set by the following written values shown in Table 2.

Table 2. Write Values Versus Analog Output Values

WriteValue (Hex) 0x0000 to 0xffff	Output Value for Each Range 0-10V	±5V	±10V
0x0000	0.0000V	-5.0000V	-10.000V
⋮	⋮	⋮	⋮
0x4000	2.5000V	-2.5000V	-5.0000V
⋮	⋮	⋮	⋮
0x8000	5.0000V	0.0000V	0.0000V
⋮	⋮	⋮	⋮
0xc000	7.5000V	2.5000V	5.0000V
⋮	⋮	⋮	⋮
0xffff	9.9999V	5.9999V	9.99998V

3. Performing Analog Output Conversions.

Four channels of 16-bit analog outputs are updated as follows.

a. DAC0 (Channel 0).

The output of DAC0 is set by writing the desired offset binary value to Base Address + 0x00.

b. DAC1 (Channel 1).

The output of DAC1 is set by writing the desired offset binary value to Base Address + 0x02.

c. DAC0 (Channel 2).

The output of DAC2 is set by writing the desired offset binary value to Base Address + 0x04.

d. DAC0 (Channel 3).

The output of DAC3 is set by writing the desired offset binary value to Base Address + 0x06.

4. Gain and Offset Adjustments.

The gain and offset values of the four outputs can be adjusted by the onboard potentiometers given in Table 3.

Table 3. Gain and Offset Potentiometer Designations

Channel	Gain Potentiometer	Offset Potentiometer
DAC0	R27	R28
DAC1	R29	R30
DAC2	R31	R32
DAC3	R33	R34

D. Analog Input Channels

1. Analog Input Range Selection.

The analog input channels have two selectable ranges of 0-5V or 0-10V installing 0.1 inch jumpers on JP6 for channels 0 (AIN0) thru 3 (AIN3) as shown in Table 4 for each channel. Note that the 0-5V range is selected if no jumper is installed and an installed jumper selects the 0-10V range for the chosen channel.

Table 4. Input Range Selection Using JP6.

CHANNEL	RANGE	INSTALL JP6 JUMPERS
AIN0	0-5V/0-10V	NONE /1,2
AIN1	0-5V/0-10V	NONE /3,4
AIN2	0-5V/0-10V	NONE /5,6
AIN3	0-5V/0-10V	NONE /7,8

2. Analog Input Addresses.

The four analog analog input channels available are AIN0 thru AIN3 with I/O addresses as shown in Table 5.

Table 5. Analog Input Addresses

Channel	I/O Address	Start Convert	Status
AIN0	Base + 0x08	Base + 0x0a	Base + 0x0c
AIN1	Base + 0x08	Base + 0x0a	Base + 0x0c
AIN2	Base + 0x08	Base + 0x0a	Base + 0x0c
AIN3	Base + 0x08	Base + 0x0a	Base + 0x0c

3. Performing Analog Input Conversions.

Conversions are performed by a read and write I/O word sequence for the desired input channel as given above. Conversions are performed by the following steps.

a. I/O word write containing the channel number to the **Start Convert** address to set the channel address. Channel numbers are 0 for AIN0, 1 for AIN1, 2 for AIN2 and 3 for AIN3.

b. Input the **Status** address of the converter until bit 0 of the status word is 1.

c. Repeat Step 1 above (exactly the same) to start the conversion.

d. Repeat Step 2 above (exactly the same) to get the status.

e. Read the input word at **I/O Address**. The 4 most significant bits of the word are ignored.

The values read are binary with 0x000 denoting 0V and 0xfff being +5V or +10V for ranges of 0-5V or 0-10V, respectively. A simple program written to test the card is given in section III below. Schematics are in section V11.

III. Simple 'C' Test Program for the MSI-P450.

```
/* Program to test P450 Analog Card - 11/01/2015 */

   char buffer[10], b;
   int baddr, csdac0, csdac1, csdac2, csdac3, csadc, stconv, status, n;

clear_screen()
    {
       char a;
       for (a=1; a<=25; a=a+1)
          printf("\n");
    }
main()
{
   baddr = 0x300;
   clear_screen();
   printf("\nInsert JP1-A8, JP1-A9 for Base Addr = 0x300.\n");
   gets(buffer);
   clear_screen();
   csdac0 = baddr;
   csdac1 = baddr + 0x2;
   csdac2 = baddr + 0x4;
   csdac3 = baddr + 0x6;
   csadc  = baddr + 0x8;
   stconv = baddr + 0xA;
   status = baddr + 0xC;
start:

/* Tests the ADC's */

   printf("\nApply test voltages to TS3-1, 3, 5, & 7.\n");
   gets(buffer);
start1:
   printf("Enter ADC input channel (7 to goto DAC's) = ");
   gets(buffer);
   b = buffer[0];
   if(b == 0x30)
```

```
{
    outportw(stconv, 0x0000);/* send set address write */
    while((inportw(status) & 1) == 0);
    outportw(stconv, 0x0000);/* send start conversion write */
    while((inportw(status) & 1) == 0);
    printf("Value of Chan 0 = ");
    printf("%X\n", inportw(csadc) & 0xfff);/* read chan 0 */
}
else if(b == 0x31)
{
    outportw(stconv, 0x0001);/* send set address write */
    while((inportw(status) & 1) == 0);
    outportw(stconv, 0x0001);/* send start conversion write */
    while((inportw(status) & 1) == 0);
    printf("Value of Chan 1 = ");
    printf("%X\n", inportw(csadc) & 0xfff);/* read chan 1 */
}
else if(b == 0x32)
{
    outportw(stconv, 0x0002);/* send set address write */
    while((inportw(status) & 1) == 0);
    outportw(stconv, 0x0002);/* send start conversion write */
    while((inportw(status) & 1) == 0);
    printf("Value of Chan 2 = ");
    printf("%X\n", inportw(csadc) & 0xfff);/* read chan 2 */
}
else if(b == 0x33)
{
    outportw(stconv, 0x0003);/* send set address write */
    while((inportw(status) & 1) == 0);
    outportw(stconv, 0x0003);/* send start conversion write */
    while((inportw(status) & 1) == 0);
    printf("Value of Chan 3 = ");
    printf("%X\n", inportw(csadc) & 0xfff);/* read chan 3 */
}
else if (b == 0x37)
{
     goto start2;
```

```
   }
  gets(buffer);
  goto start1;

/* Test the DAC's */

start2:
  clear_screen();
   printf("\nTest TS2-1, 3, 5, & 7 for 0V for the power-on reset
condition.\n");
  gets(buffer);
   printf("\nTest TS2-1, 3, 5, & 7 for -10.00V.\n");
  outportw(csdac0, 0x000);/* set outputs to -10V\n");*/
  outportw(csdac1, 0x000);/* set outputs to -10V\n");*/
  outportw(csdac2, 0x000);/* set outputs to -10V\n");*/
  outportw(csdac3, 0x000);/* set outputs to -10V\n");*/
  gets(buffer);
   printf("\nTest TS2-1, 3, 5, & 7 for 0.00V & adjust offsets of R28,
R30, R32 & R34.\n");
  outportw(csdac0, 0x8000);/* set outputs to 0V\n");*/
  outportw(csdac1, 0x8000);/* set outputs to 0V\n");*/
  outportw(csdac2, 0x8000);/* set outputs to 0V\n");*/
  outportw(csdac3, 0x8000);/* set outputs to 0V\n");*/
  gets(buffer);
   printf("\nTest TS2-1, 3, 5, & 7 for +10.00V & adjust gains of R27,
R29, R31 & R33.\n");
  outportw(csdac0, 0xffff);/* set outputs to 0V\n");*/
  outportw(csdac1, 0xffff);/* set outputs to 0V\n");*/
  outportw(csdac2, 0xffff);/* set outputs to 0V\n");*/
  outportw(csdac3, 0xffff);/* set outputs to 0V\n");*/
  gets(buffer);
  goto start;
}
```

IV. SPECIFICATIONS

PC/104 16-bit, stackthrough

PC/104 Data Bus 16-bit

Analog Inputs

Channels	4
Converter	ADS7842E
Inputs	Single-ended
Ranges	0-5V, 0-10V
Resolution	12 bits
Clock Freq.	2 MHz
Conversion Time	6 us maximum
Non-linearity	±1 LSB
Offset Error	±3 LSB
Gain Error	±4 LSB
Signal-to-Noise	71 dB typical
Input Impedance	249kOhm (0-5V)

Analog Outputs

Channels	Up to 4
Converter	DAC7741Y
Outputs	Single-ended
Ranges	0-10V, ±5V, ±10V
Resolution	16 bits
Non-linearity	±6 LSB maximum
Offset Error	±0.1 % of FSR
Gain Error	±0.4 % of FSR
Settling Time to ±0.003%	2 us
Reference Voltage	10V Internal
Output Current	±5 mA
Output Impedance	0.1 Ohm Typical

I/O Connectors

Input	30310-5002-HB or eq.
Output	30310-5002-HB or eq.

Option Jumpers

Address & Input Range	0.025" square posts,
Analog Output Range	0.5mm square post, 2mm grid

Electrical & Environmental

+5V @ 300 mA typical, 4 Input & 4 Output Channels

-40° to 85°C Operating Temperature

Standard Models:

MSI-P450	4 Input/4 Output Channels
MSI-P450-4-3	4 Input/3 Output Channels
MSI-P450-4-2	4 Input/2 Output Channels
MSI-P450-4-1	4 Input/1 Output Channels
MSI-P450-0-4	0 Input/4 Output Channels
MSI-P450-0-3	0 Input/3 Output Channels
MSI-P450-0-2	0 Input/2 Output Channels
MSI-P450-0-1	0 Input/1 Output Channels

APPENDIX

Circuit Diagrams

MSI-P450	see P450-1.pdf, P450-2.pdf and P450-3.pdf

Converter Documents

ADS7842E PDF Document	see ADS7842E.PDF
DAC7741 PDF Document	see DAC7741.PDF